Master’s in Telecommunications Program (ENTS)

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Name:\_\_\_\_\_\_Simran Kaur\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_   UID: \_\_\_\_116326148\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Email:\_\_\_\_\_simran94@terpmal.umd.edu\_\_\_\_\_\_\_\_\_\_ phone: \_\_\_\_\_+1(313)367-8195\_\_\_\_\_\_\_\_\_

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LDPC Codes in 5G-NR

Simran Kaur

UID #116326148

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**Abstract**

In the digital communication system, for error-free and reliable communication we use error correction codes with soft-decision algorithms. 3GPP (3rd Generation Partnership Project) has defined certain requirements for 5G-NR (New Radio) that should provide high-speed, high reliable and low latency communication among enhanced Mobile Broadband (eMBB), Ultra Low Latency Communication (URLLC) and massive Machine Type Communication (mMTC)[1]. For such purposes, 3GPP has defined new forward error-correction (FEC) coding in 5G-NR standards for both control and data channels. As we know, 4G has adopted turbo codes but at higher code rates, it gives errors. Therefore, to support type #2/#3, multiple code rates and block-length, 3GPP has adopted LDPC (Low Density Parity Check) codes in 5G-NR for data channels and Polar codes for control channels. In this paper, LDPC codes in 5G-NR have been discussed and their performance comparison with turbo codes in terms of BLER (Block Error Rate) and Es/N0.

**I. Introduction**

5G was introduced in release-15 by 3GPP with three use cases: eMBB, URLLC and mMTC. 5G - NR is not only a new generation for cellular networks to provide high speed networks but it has also been standardized to promise high-reliable, low-power consumption and low latency connections. Users these days don’t just require high speed but also a good connection (highly reliable connection) that won’t disrupt their activities. Apart from this, 5G-NR will also model a low-latency(lag-free) connection which would enable massive IoT (internet of things) network and self-driving vehicles. Hence, 3GPP has introduced LDPC coding for data channel and Polar codes for control channel in 5G-NR. LDPC coding scheme is already being used in other wireless standards such as, Wi-MAX, DVB (Digital video broadcast), ATSC (Advanced Television Committee) and IEEE Wi-Fi standards [2]. The LDPC codes used in these wireless standards are not the same as 5G because the latter has different set of requirements for its performance.

Robert G. Gallager founded the LDPC codes a decade ago in 1962. Due to required computational efforts for its calculations, they were neglected at that time. DSPs these days are fairly efficient for fast mathematical calculations. Hence LDPC codes came into picture again. LDPC codes are linear block codes, the high bits (1’s) in the matrix are low in count and they are sparse in the entire matrix. LDPC and Turbo codes are decoded using iterative/recursive algorithms and hence, their visualization using graphs are beneficial. Such graphs are called as Tanner graphs [4]. A basic idea of modeling a long complex equation into multiple smaller equations is represented in these graphs. The Tanner graph shows how data bits are combined to form a codeword. LDPC codes in 5G-NR enable different coding rates and code-block lengths. Therefore, LDPC codes are suitable for targeting peak data rates of 20Gb/s in DL (downlink) and 10Gb/s in UL(Uplink) in 5G [5].

In non-coded systems with coding rate as 1bit/symbol, we can measure the performance with measuring the SNR. The channels experiencing noise and interference require bit-encoding and in such a case, we measure the performance using BER or BLER and Eb/N0. For mMTC and URLLC, the BLER should be very low and we can’t have multiple re-transmission as we need low latency. Turns out, LDPC works close to Shannon’s limit with the method of puncturing and shortening to achieve the requirements of 5G. Shortening is the zero-padding in message bits.

The rest of the paper is organized as follows: Section II will talk about LDPC codes and their construction elements. Section III will be about LDPC code design details in 5G-NR. Performance results will be talked about in Section IV. Finally, Section V will conclude the paper.

**II. LDPC Codes**

Error correcting codes (ECC) with longer codes provide high coding gains. In a linear block encoded system, *k* bits are encoded into *n* bit long codeword. A code is made of all set of codewords. The original message is encoded in this *n* bit long code block in such a way that the initial *k* bits are followed by *n-k* parity bits. This is called systematic linear code where the input message is embedded into codeword. The above mentioned codeword is said to be of order (n,k). Total number of codewords from k bits will be of . The coding rate here will be defined as . Figure 1, a represents a basic layout of linear block encoding is in a digital communication system.

Systematic Encoder

R = 4/7

Figure 1: Systematic Encoding of k bits into n bits

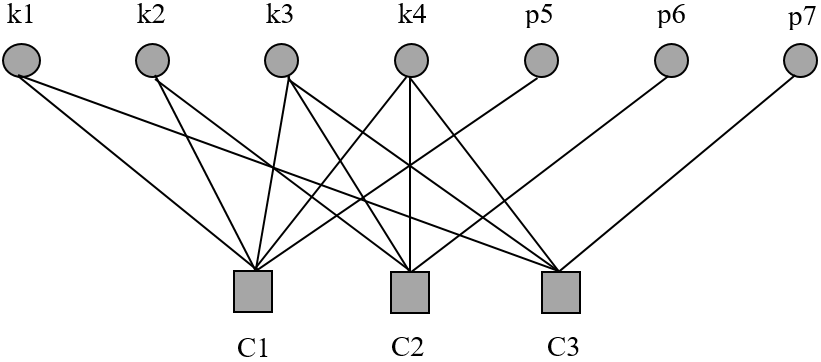
In the above figure, 4 bits are encoded into 7 bits where [p0 p1 p2] are parity bits. The design of these parity bits is in such a way that each parity bit is a modulo-2 addition (a.k.a XOR) of subset of *k* input bits. As an example, we can define , and . These equations can be represented in form of matrix where,

[] = []

If we solve above matrix, we will get our original parity bit equations. Note that the is formed by , that means the column in right side of input matrix will be . Same will be true for other parity bits. From this, we can make two very important matrices to describe LDPC codes. These are Generator matrix (G) and Parity Check Matrix (PCM). Generator matrix GkXn will give us a codeword of length *n* in a systematic manner. G is made of Identity matrix I of order and parity matrix of order . The standard equation for codeword comes as where *k* is input bit matrix and . From the above matrix representations, we can make two crucial relationships: and . Here, H is the parity check matrix and one can define the constraints using these equations to solve for input bits in a decoder. H can be defined in the form of (PT | I). PCM is a binary matrix.

The relationship needs to be satisfied to check the validity of a codeword. In other words, if each row of H multiplied by column of CT and it equals to zero, then the codeword belongs to that code.

As explained earlier, the LDPC codes can be represented using Tanner Graphs where a set of variable bits are mapped to check nodes. The columns of H matrix are termed as bit nodes while the rows of H matrix are termed as check nodes.



edge

Figure 2: Tanner graph for matrix H

Each check node can be called as Single Parity Check (SPC) code. From the Figure 2, we can easily visualize that each SPC is a modulo-2 addition of at least 1 parity bit. This applies for systematic LDPC code in which the parity bits and check node has only one edge. For an un-systematic LPDC encoding, a parity bit must appear two times in a check node. This visualization is helpful in decoding because one can decode entire LDPC matrix by solving SPC to obtain parity bits from message bits. This is further explained for 5G LDPC codes in the Section III.

The performance of LDPC codes can be described by degree distribution of the LDPC codes. The code rate depends upon the degree of the check nodes and variable bit nodes. The weight of columns, i.e., number of 1’s in a column is called as degree of variable bit node and weight of rows, i.e., number of 1’s in a row is called as degree of check node . In case of regular LDPC codes, the degrees are constant. If the weights are different, we can call such codes as irregular LDPC codes. Wireless standards have designed irregular LDPC codes with degree-2 variable nodes [6] and puncturing to improve performance and rate matching [7].

LDPC decoders can be designed using SPC decoder and repetition decoder combined and using this combination iteratively. For repetition decoder, we generally use log-likelihood ratio values of the all the received bits in codeword to detect and correct the error. The SPC is a linear block code of order (n, n-1) and number of 1’s in codeword are even. Its G consist of identity matrix of order (n-1) appended with a column of all 1’s. This will give H: a row matrix of all 1’s. As explained earlier, if we decode these separate SPC with these simple calculations, we can easily decode our parity bits. The number of iterations used to decode a codeword is limited, so if the SNR is worse, there is a possibility that the decoded codeword has errors.

**III. LDPC code design in 5G-NR**

LDPC codes are being used by different wireless standards already. The structure of LDPC codes defined depends upon the requirements and mandate of the wireless standards. 5G-NR requires the channel coding to support type #2/#3 HARQ, multiple coding rates and block lengths with less encoding/decoding complexity. This also needs to be achieved in scenarios of low SNR to give low BLERs.

LDPC in 5G-NR are designed by 3GPP based on specific requirements. LDPC code matrix in 5G-NR is based on *protographic* construction. Protograph is a smaller graph that is repeated in a specific way to create a PCM for 5G-NR LDPC codes. This is also called as base matrix or base graph (BG). Typically, the entries of base graph are expanded/lifted by right shifted matrices. This is how *sparseness* is defined and is very specific in nature. All the wireless standards have their own base matrix configurations. The ensuing LDPC codes with these cyclic shifts are of quasi-cyclic type. The expansion is explained further. We need a quasi-cyclic shifted structure for the sanity of parallelism which is very beneficial in decoding algorithms.

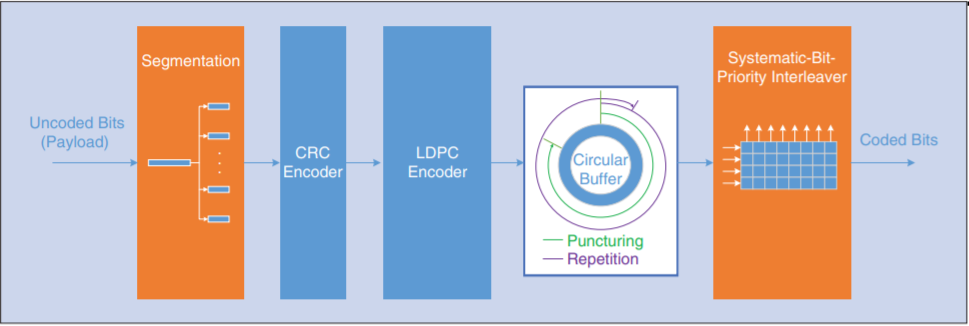


Figure 3: A basic LDPC encoding flow-diagram [5]

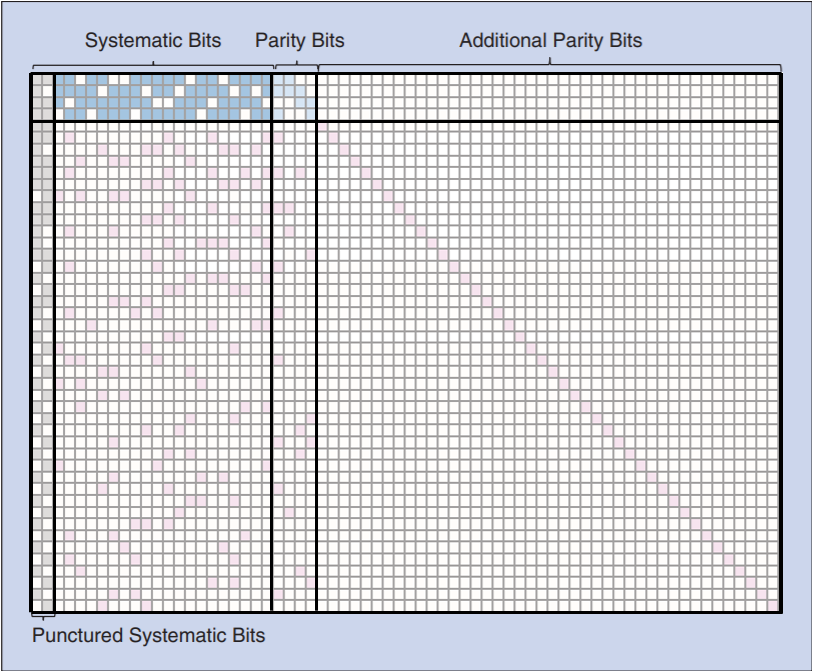
Figure 3 gives us a basic layout of encoding LDPC code. Serial uncoded bits or message bits are segmented into smaller chunks called blocks that can be processed by LDPC hardware processor. Having said that, LDPC hardware processors have “*X”* number ofprocessors working in parallel to encode and decode and the block size needs to be compatible with the number of hardware processors [2]. To improve the performance of LDPC codes, we add 24-bit cyclic-redundancy-check (CRC) [7] with every block for error detection purposes. The puncturing is done to further increase the performance without decreasing the code-rate. Puncturing is done in both message bits and parity bits in codewords. The interleaver is designed in such a way that it makes the systematic bits more reliable than other parity bits. Then the output of these blocks is combined for further PHY layer processing.

3GPP has defined 2 base matrices for LDPC codes. These base matrices are of very big in order. The first base matrix, BG1 is of order 46x68 and the second base matrix, BG2 is of order 42x52. To understand the base matrix of 5G-NR properly, we need to understand the lifting or expansion rules of *protograph* or *base matrix.* A set index *i*LS and lifting sizes Z is defined by 3GPP standards. Values for *i*LS = 0,1,2,3,4,5,6,7. The two lifting controlling factors are A = {2,3,5,7,11,13,15} and j = {0, 1, …} such that Z is in range 2 to 384. Table 1 shows all the possible values for *i*LS and corresponding values of Zc. Here we can see that Zc = Ax2j.

|  |  |
| --- | --- |
| *Set index (**)* | *Set of lifting sizes (**)* |
| 0 | {2, 4, 8, 16, 32, 64, 128, 256} |
| 1 | {3, 6, 12, 24, 48, 96, 192, 384} |
| 2 | {5, 10, 20, 40, 80, 160, 320} |
| 3 | {7, 14, 28, 56, 112, 224} |
| 4 | {9, 18, 36, 72, 144, 288} |
| 5 | {11, 22, 44, 88, 176, 352} |
| 6 | {13, 26, 52, 104, 208} |
| 7 | {15, 30, 60, 120, 240} |

Table 1: LDPC lifting values for set index [5]

The entries of the base matrix are replaced by an expansion factor or lifting value, *Zc* in a certain manner. Each entry which is “0” in base matrix, is replaced by a zero matrix of order . Similarly, each entry which is non-zero or “1” in base matrix, is replaced by a circular shift of identity matrix I of order and the shift is defined by Pi,j, where *i* and *j* are the row and column indices of that entry. For understanding and simplicity, both the matrices can be divided into smaller block structure as shown in Figure 4.



**E**

**I**

**B**

**O**

**A**

Figure 4: Base Matrix for 5G, adapted from [5]

The block configuration is as follows: **A** block is a sub matrix which is used for highest code rate. It is of dimension 4x22 for BG1 and 4x10 for BG2. It contains message part and known as systematic bits. Note that the 22 and 10 value correspond to the bit part and 4 corresponds to the rows. **E** is one of the most important sub-matrix or blocks. It contains parity bits and is of order 4x4 for both the base matrices. It has a double diagonal structure as shown in Figure 5. The **O** block is left with all zeros. The left most two columns are punctured systematic bits. These are highly dense like block **A** and is never transmitted. The double diagonal structure of block **E** is important in encoding because if we add (modulo-2) the rows of blocks **A,E** and **O** in which **A** has message part, **E** and **O** has parity part, we can easily find the first parity bit and then with iterative decoding, we can find other parity bits with the help of first parity bit.



p4

p1

p2

p3

Figure 5: Block E double diagonal

In LDPC codes, the decoding complexity is lower than the Turbo codes. This is with the fact that LDPC codes in 5G are quasi-cyclic in nature. In augmentation to reasons of low complexity, another concept of *row-orthogonality* comes into picture. Row orthogonality basically means that if we take transpose of one row, then its dot product with the other row should be zero. In 5G-NR LDPC base matrices, we can see that apart from block A, a few rows below block A and punctured columns, there are no two consecutive rows with non-zero columns [7]. In other words, core-graph can’t have orthogonality but for low latency decoding, this approach can be adopted in low-rate sub matrices. Hence the structure is also called quasi-row orthogonal.

Talking about rate, 3GPP has defined a range of block length for certain base matrices. BG1 is for higher code rates with maximum block length of 8448. BG2 is used for code rates between 1/5 ≤ R ≤ 2/3 with maximum block length of 3840 [5]. Figure 6 shows a compact description of in what ranges of rates R and block lengths K, which base matrix should be used. For block lengths less than 308 (marked in yellow), only BG2 is used. For block lengths 308 ≤ R ≤ 3840 (marked in blue), BG2 is used up to code rate 0.67, then BG1 is used for code rates till 0.95. For block lengths larger than 3840 (marked in green), BG2 is used for code rates 0.25 and for higher code rates, BG1 is used.

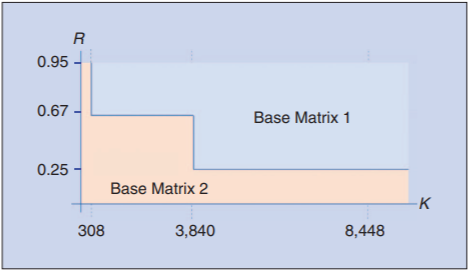


Figure 6: BG1 and BG2 matrix usage for K block lengths, adopted from [5]

**IV. Performance**

This paper explains how LDPC codes can achieve high-reliability, low-latency and lower BLERs while desired code rates. Performance depends upon the decoding complexity of the LPDC codes. As explained above, overall LDPC decoder is a combination of repetition LLR and SPC decoder and hence performance is based on how these combined decoders works in a defined channel model. The performance is calculated with respect to the BLER and Es/N0 (dB). Es/N0 is taken into consideration here because after the encoding, we are supposed to calculate the energy of the symbol rather than bits. Figure 7 shows a performance graph for 5G LDPC codes with quadrature phase shift keying (QPSK) modulation schemes applied on block length, K = 6000 in an AWGN channel. The performance of Turbo codes in LTE are put in comparison with LDPC codes in 5G while keeping all other parameters same. The decoding algorithms used here are ideal for both the codes. We can observe that for each code rate, LDPC codes have lesser BLERs as compared with Turbo codes. In other words, the higher coding gains can be achieved by LDPC codes.

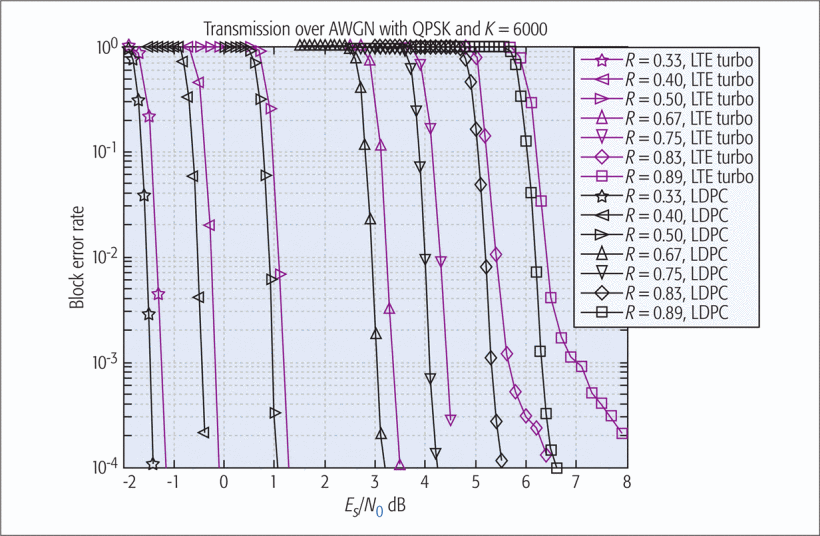


Figure 7: Performance of LDPC codes with respect to Turbo codes for block length 6000 and QPSK modulation in AWGN channel [2]

**V. Conclusion**

This paper describes the basics of LDPC codes and their adaptation in 5G-NR standards. The requirements of 5G-NR are being served by the selected LDPC codes. LDPC codes have an upper hand on Turbo codes for longer block codes in terms of performance and decoding complexity. LDPC coding could be the much-needed backbone of 5G NR which could reach Shannon’s limit when operated in certain specific configurations.

**VI. References**

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